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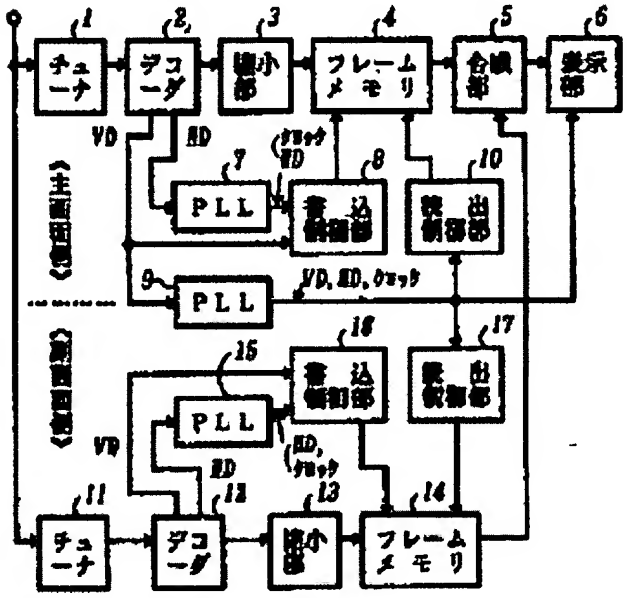
Abstract:
PROBLEM TO BE SOLVED: To prevent synchronization of sub screens from being disturbed even when synchronization of the main screen of multi-screens is disturbed. SOLUTION: Broadcasting to be a main screen is received by a tuner 1 and video signals separated in a decoder 2 are reduced to a main screen size in a reduction part 3 and written to a frame memory 4 by a write control part 8 in response to signals from a PLL 7. Plural pieces of broadcasting to be sub screens are

successively received by a tuner 11 and video signals separated in a decoder 12 are respectively reduced to a sub screen size in a reduction part 13 and written to a specified position of a frame memory 14 by a write control part 16 in response to signals from a PLL 15. Clocks, HD and VD are generated in a PLL 9 based on HD (vertical synchronizing signals) from the decoder 2, and by using the signals, signals of the frame memory 4 are read by a read control part 10, signals of a frame memory 14 are read by a read-out control part 17, they are synthesized in a synthesis part 5 and the multi-screen is displayed at a display part 6.



JPO Machine translation abstract:
(57) **Abstract**
SUBJECT Even if the synchronization of the main screen of a multi screen is confused, the synchronization of a sub-screen is made not to be disturbed.
Means for Solution Receive broadcast which serves as a main screen with the tuner 1, and a video signal separated by the decoder 2 is reduced to main screen size by the reducing part 3, It writes in the frame memory 4 by the write control part 8 by a signal from PLL7, Two or more broadcasts which serve as a sub-screen with the tuner 11 are received one by one, a video signal separated by the decoder 12 is reduced to sub-screen size by the reducing part 13, respectively, and it writes in a required position of the frame memory 14 by the write control part 16 by a signal from PLL15. Based on HD (Vertical Synchronizing signal) from the decoder 2, by PLL9 A clock, HD and VD are generated, using these signals, a signal of the frame memory 4 is read by the read-out control section 10, a signal of the frame memory 14 is read by the read-out control section 17, it compounds by the synchronizer 5, and a multi screen is displayed on the indicator 6.

Claim(s)
Claim 1 It has 2 sets of decoders which decode a signal from a tuner and a tuner which receives television broadcasting, A clock generated in the 1st PLL circuit based on a Horizontal Synchronizing signal which received broadcast which serves as a main screen with the 1st tuner, reduced a video signal from the 1st decoder to necessary size by the 1st reducing part, and was

separated by the 1st decoder, It writes in the 1st frame memory via the 1st write control part with a Horizontal Synchronizing signal and a Vertical Synchronizing signal from the 1st decoder, Two or more broadcasts which switch the 2nd tuner with a necessary time interval, and serve as a sub-screen are received, A clock generated in the 2nd PLL circuit based on a Horizontal Synchronizing signal which reduced each video signal from the 2nd decoder to necessary size by the 2nd reducing part, respectively, and was separated by the 2nd decoder, It writes in a required position of the 2nd frame memory via the 2nd write control part, respectively with a Horizontal Synchronizing signal and a Vertical Synchronizing signal from the 2nd decoder, In what compounds a video signal read via the 1st read-out control section from said 1st frame memory, and a video signal read via the 2nd read-out control section from the 2nd frame memory by a synchronizer, and displays a multi screen by an indicator, On a basis a Vertical Synchronizing signal from said 1st decoder A clock, A multi screen display device which provides the 3rd PLL circuit that generates a Horizontal Synchronizing signal and a Vertical Synchronizing signal, and was made to read a video signal from said 2nd frame memory with a clock, and a Horizontal Synchronizing signal and a Vertical Synchronizing signal from the 3rd PLL circuit via the 2nd read-out control section.

Claim 2 The multi screen display device according to claim 1 which was made to read a video signal from said 1st frame memory with a clock, and a Horizontal Synchronizing signal and a Vertical Synchronizing signal from said 3rd PLL circuit via the 1st read-out control section.

Claim 3 The multi screen display device according to claim 1 or 2 which was made to control said indicator by clock, and a Horizontal Synchronizing signal and a Vertical Synchronizing signal from said 3rd PLL circuit.

Claim 4 When said 3rd PLL circuit is supervised in timing of a self-propelled Vertical Synchronizing signal which generated a Vertical Synchronizing signal from said 1st decoder based on a self-propelled clock and a Vertical Synchronizing signal from the 1st decoder is not distinguished, a self-propelled clock, The multi screen display device according to claim 1, 2, or 3 which comes to be what outputs a Horizontal Synchronizing signal and a Vertical Synchronizing signal which were generated based on a self-propelled clock.

Detailed Description of the Invention

0001

Field of the Invention This invention relates to a multi screen display device, and when the synchronization of the inputted video signal used as a main screen is confused, it relates to the thing keep the synchronization of a sub-screen from being confused.

0002

Description of the Prior Art2 sets of decoders which decode the signal from a tuner and a tuner which receives television broadcasting are provided, and some which were constituted like the example shown in the block diagram of drawing 3 are shown in the multi screen display device which displays two or more screens simultaneously. Receive the broadcast which serves as a main screen with the tuner 1, and by the decoder 2 Namely, a video signal, Decode to a Horizontal Synchronizing signal (HD) and a Vertical Synchronizing signal (VD), and a video signal is reduced by the reducing part 3, Write in the frame memory 4 by the signal from the write control part 8, and simultaneously, with a required interval, switch a channel and two or more broadcasts which serve as a sub-screen with the tuner 11 are received, Decode to a video signal, and HD and VD by the decoder 12, and a video signal is reduced to necessary size by the reducing part 13, It writes in the required position of the frame memory 14 one by one by the signal from the write control part 16, the video signal of a main screen and the video signal of a sub-screen which were read from the frame memories 4 and 14 by the signal from the read-out control sections 21 and 22 are compounded by the synchronizer 5, and it displays by the indicator 6. The read-out control section 21 and the read-out control section 22 perform read-out from the frame memory 4 and the frame memory 14 by HD and the clock which were synchronized with HD from the decoder 2 in PLL circuit 7, and were generated, and VD from the decoder 2, and This sake, When the synchronization of a main screen is confused or it breaks off, in order that VD from the decoder 2 may confuse or break off, even when there is no disorder in the synchronized signal from the decoder 12, the synchronization of the signal read from the frame memory 14 is confused, and there is a problem

that the synchronization of the indicator 6 is disturbed simultaneously.

0003

Problem(s) to be Solved by the Invention When this invention does not have disorder of a synchronization in the video signal of a sub-screen in view of such a point, even if disorder of the synchronization with the video signal of a main screen arises, the sub-screen of a multi screen at least aims at making it displayed without confusing a synchronization.

0004

Means for Solving the Problem In order to attain the above-mentioned purpose, in a multi screen display device of this invention. It has 2 sets of decoders which decode a signal from a tuner and a tuner which receives television broadcasting, A clock generated in the 1st PLL circuit based on a Horizontal Synchronizing signal which received broadcast which serves as a main screen with the 1st tuner, reduced a video signal from the 1st decoder to necessary size by the 1st reducing part, and was separated by the 1st decoder, It writes in the 1st frame memory via the 1st write control part with a Horizontal Synchronizing signal and a Vertical Synchronizing signal from the 1st decoder, Two or more broadcasts which switch the 2nd tuner with a necessary time interval, and serve as a sub-screen are received, A clock generated in the 2nd PLL circuit based on a Horizontal Synchronizing signal which reduced each video signal from the 2nd decoder to necessary size by the 2nd reducing part, respectively, and was separated by the 2nd decoder, It writes in a required position of the 2nd frame memory via the 2nd write control part, respectively with a Horizontal Synchronizing signal and a Vertical Synchronizing signal from the 2nd decoder, In what compounds a video signal read via the 1st read-out control section from said 1st frame memory, and a video signal read via the 2nd read-out control section from the 2nd frame memory by a synchronizer, and displays a multi screen by an indicator, Provide the 3rd PLL circuit that generates a clock, a Horizontal Synchronizing signal, and a Vertical Synchronizing signal based on a Vertical Synchronizing signal from said 1st decoder, and A clock from the 3rd PLL circuit, A video signal is read from the 2nd frame memory via the 2nd read-out control section with a Horizontal Synchronizing signal and a Vertical Synchronizing signal.

0005A video signal of the 1st frame memory is read via the 1st read-out control section with a clock, and a Horizontal Synchronizing signal and a Vertical Synchronizing signal from said 3rd PLL circuit.

0006 And said indicator is controlled by clock, and a Horizontal Synchronizing signal and a Vertical Synchronizing signal from said 3rd PLL circuit.

0007 When said 3rd PLL circuit is supervised in timing of a self-propelled Vertical Synchronizing signal which generated a Vertical Synchronizing signal from the 1st decoder based on a self-propelled clock and a Vertical Synchronizing signal from the 1st decoder is not distinguished, a self-propelled clock, A Horizontal Synchronizing signal and a Vertical Synchronizing signal which were generated based on this clock are outputted.

0008

Embodiment of the Invention An embodiment of the invention is described with reference to Drawings based on working example. Drawing 1 is an important section block diagram of one working example of the multi screen display device by this invention. In a figure, it is the 1st and 2nd tuner, and 1 and 11 receive the TV broadcast which serves as a main screen with the 1st tuner 1, with a necessary time interval, they switch a channel one by one and receive the TV broadcast which serves as a sub-screen with the 2nd tuner 11. 2 and 12 are the 1st and 2nd decoder, process the composite video signal from the 1st tuner 1 or the 2nd tuner 11, and separate HD and VD. 3 and 13 are the 1st and 2nd reducing part, and reduce the video signal from the 1st decoder 2 or the 2nd decoder 12 to necessary size by infanticide of a pixel and a line, etc., respectively. 4 and 14 are the 1st and 2nd frame memory, and write in the video signal from the 1st reducing part 3 or the 2nd reducing part 13. 5 is a synchronizer and compounds the video signal read from the 1st frame memory 4 and the 2nd frame memory 14 on one screen. 6 is an indicator and displays a multi screen based on the signal from the synchronizer 5. 7 is the 1st PLL circuit, generates the clock in sync with HD from the 1st decoder 2, and generates HD based on this clock. 8 is the 1st write control part and controls the writing of the 1st frame memory 4 by VD from the clock, HD, and the 1st decoder 2 from 1st PLL circuit 7. 9 is the 3rd PLL circuit, generates a clock on the basis of VD from the 1st decoder 2, and generates HD and VD based on this clock. 10 is the 1st read-out control section, and controls read-out of the 1st frame memory 4 by the clock from 3rd PLL circuit

9, and HD and VD. 15 is the 2nd PLL circuit, generates the clock in sync with HD from the 2nd decoder 12, and generates HD based on this clock. 16 is the 2nd write control part and controls the writing of the 2nd frame memory 14 by VD from the clock, HD, and the 2nd decoder 12 from 2nd PLL circuit 15. 17 is the 2nd read-out control section, and controls read-out of the 2nd frame memory 14 by the clock from 3rd PLL circuit 9, and HD and VD.

0009 Next, operation of the multi screen display device by this invention is explained. For example, as shown in drawing 2, when compounding main screen and five sub-screen ** - ** and considering it as a multi screen, The 1st tuner 1 receives broadcast used as a main screen, and a video signal is taken out by the 1st decoder 2, Input into the 1st reducing part 3 and a line number and the pixel number of each line are reduced to 2/3 by infanticide of a line and a pixel, etc., respectively, It writes in the required position (position corresponding to the main screen of drawing 2) of the 1st frame memory 4 by the 1st write control part 8 using VD from the clock, HD, and the 1st decoder 2 from 1st PLL circuit 7, Switch each broadcast channel which becomes sub-screen **, **, **, **, and ** with the 2nd tuner 11 one by one with a necessary time interval, and it receives, Take out a video signal by the 2nd decoder 12, respectively, and it inputs into the 2nd reducing part 13, A line number and the pixel number of one line are reduced to 1/3 by infanticide of a line and a pixel, etc., respectively, It writes in the required position (position corresponding to sub-screen **of drawing 2** ** - **) of the 2nd frame memory 14 one by one by the 2nd write control part 16 using VD from the clock, HD, and the 2nd decoder 12 from 2nd PLL circuit 15. And by the 1st read-out control section 10, the image of a main screen is read from the 1st frame memory 4, the image of sub-screen ** - ** is read from the 2nd frame memory 14 by the 2nd read-out control section 17, respectively, and it compounds on one screen by the synchronizer 5, inputs into the indicator 6, and displays on a screen.

0010 The 1st and 2nd read-out control sections 10 and 17 read each frame memory using the clock from 3rd PLL circuit 9, and HD and VD. Since 3rd PLL circuit 9 generates a clock on the basis of VD from the 2nd decoder 2 and HD and VD are generated based on this clock, Naturally, although the disorder of the synchronization with read-out of the signal from each frame memory and the drive of the indicator 6 is not produced, since VD from the 2nd decoder 2 is supervised in the timing of the running by itself VD generated on the basis of a self-propelled clock, When disorder arises to the cycle of VD with the obstacle etc. which were produced in the broadcast wave and VD input is not distinguished, a clock, and self-propelled HD and VD are supplied to the 1st and 2nd read-out control sections 10 and 17. Therefore, although there is naturally disorder of a synchronization in the signal of the main screen read from the 1st frame memory 4, Since these each sub-screen can be read in the state where there is no disorder of a synchronization and the indicator 6 is simultaneously controlled by this clock when each sub-screen of the 2nd frame memory 14 is written in in the normal state of the synchronization, a sub-screen at least is displayed without confusing a synchronization.

0011 The 2nd tuner 11 makes channel selection time of sub-screen ** longer than the channel selection time of sub-screen ** - **, expresses sub-screen ** as an animation with imperfection, and expresses sub-screen ** which remains - ** as a top dropping screen, for example.

0012

Effect of the Invention As explained above, according to the multi screen display device by this invention. It is what performs read-out from each frame memory of the Lord and a sub-screen, control of an indicator, etc. using the synchronized signal generated in a PLL circuit on the basis of the Vertical Synchronizing signal of the video signal used as a main screen, Since the synchronized signal generated by running by itself in a PLL circuit is used when the synchronization of a main screen is confused or, even when the synchronization of a main screen is confused, each sub-screen is displayed without disturbing a synchronization.

Field of the Invention This invention relates to a multi screen display device, and when the synchronization of the inputted video signal used as a main screen is confused, it relates to the thing keep the synchronization of a sub-screen from being confused.

Description of the Prior Art2 sets of decoders which decode the signal from a tuner and a tuner which receives television broadcasting are provided, and some which were constituted like the example shown in the block diagram of drawing 3 are shown in the multi screen display device which displays two or more screens simultaneously. Receive the broadcast which serves as a main screen with the tuner 1, and by the decoder 2 Namely, a video signal, Decode to a Horizontal Synchronizing signal (HD) and a Vertical Synchronizing signal (VD), and a video signal is reduced by the reducing part 3, Write in the frame memory 4 by the signal from the write control part 8, and simultaneously, with a required interval, switch a channel and two or more broadcasts which serve as a sub-screen with the tuner 11 are received, Decode to a video signal, and HD and VD by the decoder 12, and a video signal is reduced to necessary size by the reducing part 13, It writes in the required position of the frame memory 14 one by one by the signal from the write control part 16, the video signal of a main screen and the video signal of a sub-screen which were read from the frame memories 4 and 14 by the signal from the read-out control sections 21 and 22 are compounded by the synchronizer 5, and it displays by the indicator 6. The read-out control section 21 and the read-out control section 22 perform read-out from the frame memory 4 and the frame memory 14 by HD and the clock which were synchronized with HD from the decoder 2 in PLL circuit 7, and were generated, and VD from the decoder 2, and This sake, When the synchronization of a main screen is confused or it breaks off, in order that VD from the decoder 2 may confuse or break off, even when there is no disorder in the synchronized signal from the decoder 12, the synchronization of the signal read from the frame memory 14 is confused, and there is a problem that the synchronization of the indicator 6 is disturbed simultaneously.

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Problem(s) to be Solved by the Invention When this invention does not have disorder of a synchronization in the video signal of a sub-screen in view of such a point, even if disorder of the synchronization with the video signal of a main screen arises, the sub-screen of a multi screen at least aims at making it displayed without confusing a synchronization.

Means for Solving the Problem In order to attain the above-mentioned purpose, in a multi screen display device of this invention. It has 2 sets of decoders which decode a signal from a tuner and a tuner which receives television broadcasting, A clock generated in the 1st PLL circuit based on a Horizontal Synchronizing signal which received broadcast which serves as a main screen with the 1st tuner, reduced a video signal from the 1st decoder to necessary size by the 1st reducing part, and was separated by the 1st decoder, It writes in the 1st frame memory via the 1st write control part with a Horizontal Synchronizing signal and a Vertical Synchronizing signal from the 1st decoder, Two or more broadcasts which switch the 2nd tuner with a necessary time interval, and serve as a sub-screen are received, A clock generated in the 2nd PLL circuit based on a Horizontal Synchronizing signal which reduced each video signal from the 2nd decoder to necessary size by the 2nd reducing part, respectively, and was separated by the 2nd decoder, It writes in a required position of the 2nd frame memory via the 2nd write control part, respectively with a Horizontal Synchronizing signal and a Vertical Synchronizing signal from the 2nd decoder, In what compounds a video signal read via the 1st read-out control section from said 1st frame

memory, and a video signal read via the 2nd read-out control section from the 2nd frame memory by a synchronizer, and displays a multi screen by an indicator, Provide the 3rd PLL circuit that generates a clock, a Horizontal Synchronizing signal, and a Vertical Synchronizing signal based on a Vertical Synchronizing signal from said 1st decoder, and A clock from the 3rd PLL circuit, A video signal is read from the 2nd frame memory via the 2nd read-out control section with a Horizontal Synchronizing signal and a Vertical Synchronizing signal.

0005A video signal of the 1st frame memory is read via the 1st read-out control section with a clock, and a Horizontal Synchronizing signal and a Vertical Synchronizing signal from said 3rd PLL circuit.

0006 And said indicator is controlled by clock, and a Horizontal Synchronizing signal and a Vertical Synchronizing signal from said 3rd PLL circuit.

0007 When said 3rd PLL circuit is supervised in timing of a self-propelled Vertical Synchronizing signal which generated a Vertical Synchronizing signal from the 1st decoder based on a self-propelled clock and a Vertical Synchronizing signal from the 1st decoder is not distinguished, a self-propelled clock, A Horizontal Synchronizing signal and a Vertical Synchronizing signal which were generated based on this clock are outputted.

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0009 Next, operation of the multi screen display device by this invention is explained. For example, as shown in drawing 2, when compounding main screen and five sub-screen ** - ** and considering it as a multi screen, The 1st tuner 1 receives broadcast used as a main screen, and a video signal is taken out by the 1st decoder 2, Input into the 1st reducing part 3 and a line number and the pixel number of each line are reduced to 2/3 by infanticide of a line and a pixel, etc., respectively, It writes in the required position (position corresponding to the main screen of drawing 2) of the 1st frame memory 4 by the 1st write control part 8 using VD from the clock, HD, and the 1st decoder 2 from 1st PLL circuit 7, Switch each broadcast channel which becomes sub-screen **, **, **, **, and ** with the 2nd tuner 11 one by one with a necessary time interval, and it receives, Take out a video signal by the 2nd decoder 12, respectively, and it inputs into the 2nd reducing part 13, A line number and the pixel number of one line are reduced to 1/3 by infanticide of a line and a pixel, etc., respectively, It writes in the required position (position corresponding to sub-screen **of drawing 2** ** - **) of the 2nd frame memory 14 one by one by the 2nd write control part 16 using VD from the clock, HD, and the 2nd decoder 12 from 2nd PLL circuit 15. And by the 1st read-out control section 10, the image of a main screen is read from the 1st frame memory 4, the image of sub-screen ** - ** is read from the 2nd frame memory 14 by

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0010 The 1st and 2nd read-out control sections 10 and 17 read each frame memory using the clock from 3rd PLL circuit 9, and HD and VD. Since 3rd PLL circuit 9 generates a clock on the basis of VD from the 2nd decoder 2 and HD and VD are generated based on this clock, Naturally, although the disorder of the synchronization with read-out of the signal from each frame memory and the drive of the indicator 6 is not produced, since VD from the 2nd decoder 2 is supervised in the timing of the running by itself VD generated on the basis of a self-propelled clock, When disorder arises to the cycle of VD with the obstacle etc. which were produced in the broadcast wave and VD input is not distinguished, a clock, and self-propelled HD and VD are supplied to the 1st and 2nd read-out control sections 10 and 17. Therefore, although there is naturally disorder of a synchronization in the signal of the main screen read from the 1st frame memory 4, Since these each sub-screen can be read in the state where there is no disorder of a synchronization and the indicator 6 is simultaneously controlled by this clock when each sub-screen of the 2nd frame memory 14 is written in in the normal state of the synchronization, a sub-screen at least is displayed without confusing a synchronization.
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Brief Description of the Drawings
Drawing 1 It is an important section block diagram of one working example of the multi screen display device by this invention.
Drawing 2 It is an example of a multi screen.
Drawing 3 It is an important section block diagram of an example of the conventional multi screen display device.
Description of Notations
1 and 11 Tuner
2 and 12 Decoder
3 and 13 Reducing part
4 and 14 Frame memory
5 Synchronizer
6 Indicator
7, 9, 15 PLL circuits
8 and 16 Write control part
10, 17, 21, and 22 Read-out control section

Drawing 1

For drawings please refer to the original document.

Drawing 2

For drawings please refer to the original document.

Drawing 3

For drawings please refer to the original document.

For drawings please refer to the original document.

PATENT ABSTRACTS OF JAPAN

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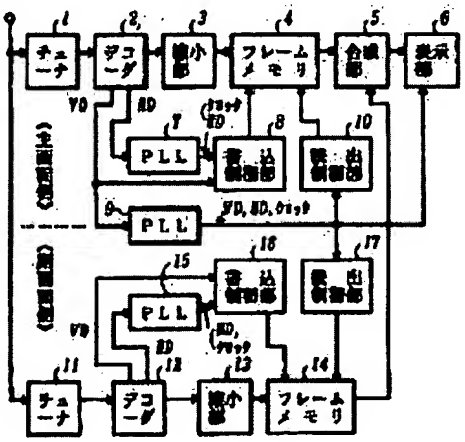
(22)Date of filing : **10.12.1997**

(71)Applicant : **FUJITSU GENERAL LTD**
(72)Inventor : **KONDO SATORU**
SHIMURA KENJI
FURUYA TOMOHIDE

(54) MULTI-SCREEN DISPLAY DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To prevent synchronization of sub screens from being disturbed even when synchronization of the main screen of multi-screens is disturbed.
SOLUTION: Broadcasting to be a main screen is received by a tuner 1 and video signals separated in a decoder 2 are reduced to a main screen size in a reduction part 3 and written to a frame memory 4 by a write control part 8 in response to signals from a PLL 7. Plural pieces of broadcasting to be sub screens are successively received by a tuner 11 and video signals separated in a decoder 12 are respectively reduced to a sub screen size in a reduction part 13 and written to a specified position of a frame memory 14 by a write control part 16 in response to signals from a PLL 15. Clocks, HD and VD are generated in a PLL 9 based on HD (vertical synchronizing signals) from the decoder 2, and by using the signals, signals of the frame memory 4 are read by a read control part 10, signals of a frame memory 14 are read by a read-out control part 17, they are synthesized in a synthesis part 5 and the multi-screen is displayed at a display part 6.



* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
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[Description of the Prior Art]2 sets of decoders which decode the signal from a tuner and a tuner which receives television broadcasting are provided, and some which were constituted like the example shown in the block diagram of drawing 3 are shown in the multi screen display device which displays two or more screens simultaneously. Receive the broadcast which serves as a main screen with the tuner 1, and by the decoder 2 Namely, a video signal, Decode to a Horizontal Synchronizing signal (HD) and a Vertical Synchronizing signal (VD), and a video signal is reduced by the reducing part 3, Write in the frame memory 4 by the signal from the write control part 8, and simultaneously, with a required interval, switch a channel and two or more broadcasts which serve as a sub-screen with the tuner 11 are received, Decode to a video signal, and HD and VD by the decoder 12, and a video signal is reduced to necessary size by the reducing part 13, It writes in the required position of the frame memory 14 one by one by the signal from the write control part 16, the video signal of a main screen and the video signal of a sub-screen which were read from the frame memories 4 and 14 by the signal from the read-out control sections 21 and 22 are compounded by the synchronizer 5, and it displays by the indicator 6. The read-out control section 21 and the read-out control section 22 perform read-out from the frame memory 4 and the frame memory 14 by HD and the clock which were synchronized with HD from the decoder 2 in PLL circuit 7, and were generated, and VD from the decoder 2, and This sake, When the synchronization of a main screen is confused or it breaks off, in order that VD from the decoder 2 may confuse or break off, even when there is no disorder in the synchronized signal from the decoder 12, the synchronization of the signal read from the frame memory 14 is confused, and there is a problem that the synchronization of the indicator 6 is disturbed simultaneously.
[0003]
[Problem(s) to be Solved by the Invention]When this invention does not have disorder of a synchronization in the video signal of a sub-screen in view of such a point, even if disorder of the synchronization with the video signal of a main screen arises, the sub-screen of a multi screen at least aims at making it displayed without confusing a synchronization.
[0004]
[Means for Solving the Problem]In order to attain the above-mentioned purpose, in a multi screen display device of this invention. It has 2 sets of decoders which decode a signal from a tuner and a tuner which receives television broadcasting, A clock generated in the 1st PLL circuit based on a Horizontal Synchronizing signal which received broadcast which serves as a main screen with the 1st tuner, reduced a video signal from the 1st decoder to necessary size by the 1st reducing part, and was separated by the 1st decoder, It writes in the 1st frame memory via the 1st write control part with a Horizontal Synchronizing signal and a Vertical

Synchronizing signal from the 1st decoder, Two or more broadcasts which switch the 2nd tuner with a necessary time interval, and serve as a sub-screen are received, A clock generated in the 2nd PLL circuit based on a Horizontal Synchronizing signal which reduced each video signal from the 2nd decoder to necessary size by the 2nd reducing part, respectively, and was separated by the 2nd decoder, It writes in a required position of the 2nd frame memory via the 2nd write control part, respectively with a Horizontal Synchronizing signal and a Vertical Synchronizing signal from the 2nd decoder, In what compounds a video signal read via the 1st read-out control section from said 1st frame memory, and a video signal read via the 2nd read-out control section from the 2nd frame memory by a synchronizer, and displays a multi screen by an indicator, Provide the 3rd PLL circuit that generates a clock, a Horizontal Synchronizing signal, and a Vertical Synchronizing signal based on a Vertical Synchronizing signal from said 1st decoder, and A clock from the 3rd PLL circuit, A video signal is read from the 2nd frame memory via the 2nd read-out control section with a Horizontal Synchronizing signal and a Vertical Synchronizing signal.

[0005]A video signal of the 1st frame memory is read via the 1st read-out control section with a clock, and a Horizontal Synchronizing signal and a Vertical Synchronizing signal from said 3rd PLL circuit.

[0006]And said indicator is controlled by clock, and a Horizontal Synchronizing signal and a Vertical Synchronizing signal from said 3rd PLL circuit.

[0007]When said 3rd PLL circuit is supervised in timing of a self-propelled Vertical Synchronizing signal which generated a Vertical Synchronizing signal from the 1st decoder based on a self-propelled clock and a Vertical Synchronizing signal from the 1st decoder is not distinguished, a self-propelled clock, A Horizontal Synchronizing signal and a Vertical Synchronizing signal which were generated based on this clock are outputted.

[0008]

[Embodiment of the Invention]An embodiment of the invention is described with reference to Drawings based on working example. Drawing 1 is an important section block diagram of one working example of the multi screen display device by this invention. In a figure, it is the 1st and 2nd tuner, and 1 and 11 receive the TV broadcast which serves as a main screen with the 1st tuner 1, with a necessary time interval, they switch a channel one by one and receive the TV broadcast which serves as a sub-screen with the 2nd tuner 11. 2 and 12 are the 1st and 2nd decoder, process the composite video signal from the 1st tuner 1 or the 2nd tuner 11, and separate HD and VD. 3 and 13 are the 1st and 2nd reducing part, and reduce the video signal from the 1st decoder 2 or the 2nd decoder 12 to necessary size by infanticide of a pixel and a line, etc., respectively. 4 and 14 are the 1st and 2nd frame memory, and write in the video signal from the 1st reducing part 3 or the 2nd reducing part 13. 5 is a synchronizer and compounds the video signal read from the 1st frame memory 4 and the 2nd frame memory 14 on one screen. 6 is an indicator and displays a multi screen based on the signal from the synchronizer 5. 7 is the 1st PLL circuit, generates the clock in sync with HD from the 1st decoder 2, and generates HD based on this clock. 8 is the 1st write control part and controls the writing of the 1st frame memory 4 by VD from the clock, HD, and the 1st decoder 2 from 1st PLL circuit 7. 9 is the 3rd PLL circuit, generates a clock on the basis of VD from the 1st decoder 2, and generates HD and VD based on this clock. 10 is the 1st read-out control section, and controls read-out of the 1st frame memory 4 by the clock from 3rd PLL circuit 9, and HD and VD. 15 is the 2nd PLL circuit, generates the clock in sync with HD from the 2nd decoder 12, and generates HD based on this clock. 16 is the 2nd write control part and controls the writing of the 2nd frame memory 14 by VD from the clock, HD, and the 2nd decoder 12 from 2nd PLL circuit 15. 17 is the 2nd read-out control section, and controls read-out of the 2nd frame memory 14 by the clock from 3rd PLL circuit 9, and HD and VD.

[0009]Next, operation of the multi screen display device by this invention is explained. For example, as shown in drawing 2, when compounding main screen and five sub-screen ** - ** and considering it as a multi screen, The 1st tuner 1 receives broadcast used as a main screen, and a video signal is taken out by the 1st decoder 2, Input into the 1st reducing part 3 and a line number and the pixel number of each line are reduced to 2/3 by infanticide of a line and a pixel,

etc., respectively, It writes in the required position (position corresponding to the main screen of drawing 2) of the 1st frame memory 4 by the 1st write control part 8 using VD from the clock, HD, and the 1st decoder 2 from 1st PLL circuit 7, Switch each broadcast channel which becomes sub-screen **, **, **, **, and ** with the 2nd tuner 11 one by one with a necessary time interval, and it receives, Take out a video signal by the 2nd decoder 12, respectively, and it inputs into the 2nd reducing part 13, A line number and the pixel number of one line are reduced to 1/3 by infanticide of a line and a pixel, etc., respectively, It writes in the required position (position corresponding to sub-screen [of drawing 2] ** - **) of the 2nd frame memory 14 one by one by the 2nd write control part 16 using VD from the clock, HD, and the 2nd decoder 12 from 2nd PLL circuit 15. And by the 1st read-out control section 10, the image of a main screen is read from the 1st frame memory 4, the image of sub-screen ** - ** is read from the 2nd frame memory 14 by the 2nd read-out control section 17, respectively, and it compounds on one screen by the synchronizer 5, inputs into the indicator 6, and displays on a screen.

[0010]The 1st and 2nd read-out control sections 10 and 17 read each frame memory using the clock from 3rd PLL circuit 9, and HD and VD. Since 3rd PLL circuit 9 generates a clock on the basis of VD from the 2nd decoder 2 and HD and VD are generated based on this clock, Naturally, although the disorder of the synchronization with read-out of the signal from each frame memory and the drive of the indicator 6 is not produced, since VD from the 2nd decoder 2 is supervised in the timing of the running by itself VD generated on the basis of a self-propelled clock, When disorder arises to the cycle of VD with the obstacle etc. which were produced in the broadcast wave and VD input is not distinguished, a clock, and self-propelled HD and VD are supplied to the 1st and 2nd read-out control sections 10 and 17. Therefore, although there is naturally disorder of a synchronization in the signal of the main screen read from the 1st frame memory 4, Since these each sub-screen can be read in the state where there is no disorder of a synchronization and the indicator 6 is simultaneously controlled by this clock when each sub-screen of the 2nd frame memory 14 is written in in the normal state of the synchronization, a sub-screen at least is displayed without confusing a synchronization.

[0011]The 2nd tuner 11 makes channel selection time of sub-screen ** longer than the channel selection time of sub-screen ** - **, expresses sub-screen ** as an animation with imperfection, and expresses sub-screen ** which remains - ** as a top dropping screen, for example.

[0012]

[Effect of the Invention]As explained above, according to the multi screen display device by this invention. It is what performs read-out from each frame memory of the Lord and a sub-screen, control of an indicator, etc. using the synchronized signal generated in a PLL circuit on the basis of the Vertical Synchronizing signal of the video signal used as a main screen, Since the synchronized signal generated by running by itself in a PLL circuit is used when the synchronization of a main screen is confused or, even when the synchronization of a main screen is confused, each sub-screen is displayed without disturbing a synchronization.

[Translation done.]

CLAIMS

[Claim(s)]
[Claim 1]It has 2 sets of decoders which decode a signal from a tuner and a tuner which receives television broadcasting, A clock generated in the 1st PLL circuit based on a Horizontal Synchronizing signal which received broadcast which serves as a main screen with the 1st tuner, reduced a video signal from the 1st decoder to necessary size by the 1st reducing part, and was separated by the 1st decoder, It writes in the 1st frame memory via the 1st write control part with a Horizontal Synchronizing signal and a Vertical Synchronizing signal from the 1st decoder, Two or more broadcasts which switch the 2nd tuner with a necessary time interval, and serve as a sub-screen are received, A clock generated in the 2nd PLL circuit based on a Horizontal Synchronizing signal which reduced each video signal from the 2nd decoder to necessary size by the 2nd reducing part, respectively, and was separated by the 2nd decoder, It writes in a required position of the 2nd frame memory via the 2nd write control part, respectively with a Horizontal Synchronizing signal and a Vertical Synchronizing signal from the 2nd decoder, In what compounds a video signal read via the 1st read-out control section from said 1st frame memory, and a video signal read via the 2nd read-out control section from the 2nd frame memory by a synchronizer, and displays a multi screen by an indicator, On a basis a Vertical Synchronizing signal from said 1st decoder A clock, A multi screen display device which provides the 3rd PLL circuit that generates a Horizontal Synchronizing signal and a Vertical Synchronizing signal, and was made to read a video signal from said 2nd frame memory with a clock, and a Horizontal Synchronizing signal and a Vertical Synchronizing signal from the 3rd PLL circuit via the 2nd read-out control section.
[Claim 2]The multi screen display device according to claim 1 which was made to read a video signal from said 1st frame memory with a clock, and a Horizontal Synchronizing signal and a Vertical Synchronizing signal from said 3rd PLL circuit via the 1st read-out control section.
[Claim 3]The multi screen display device according to claim 1 or 2 which was made to control said indicator by clock, and a Horizontal Synchronizing signal and a Vertical Synchronizing signal from said 3rd PLL circuit.
[Claim 4]When said 3rd PLL circuit is supervised in timing of a self-propelled Vertical Synchronizing signal which generated a Vertical Synchronizing signal from said 1st decoder based on a self-propelled clock and a Vertical Synchronizing signal from the 1st decoder is not distinguished, a self-propelled clock, The multi screen display device according to claim 1, 2, or 3 which comes to be what outputs a Horizontal Synchronizing signal and a Vertical Synchronizing signal which were generated based on a self-propelled clock.

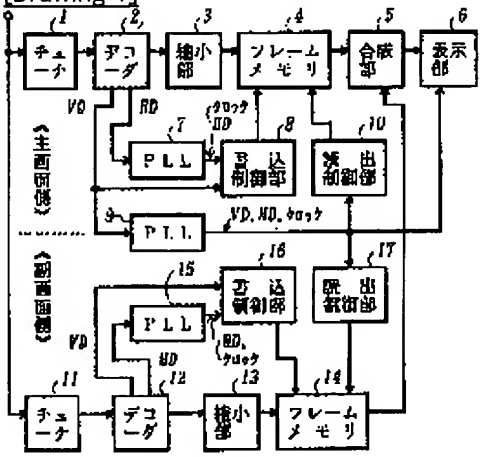
[Translation done.]

* NOTICES *

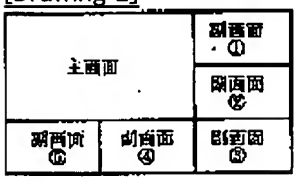
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

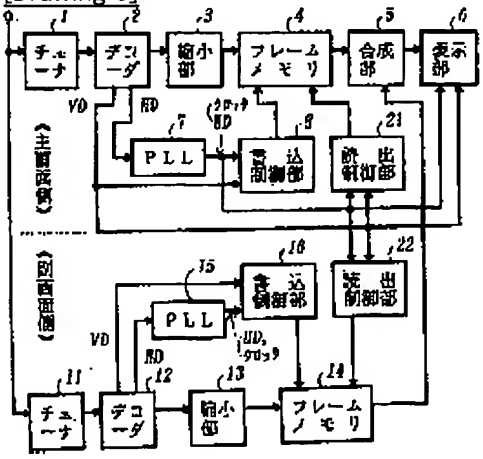
[Drawing 1]



[Drawing 2]



[Drawing 3]



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					５５０Ｒ
	5/14			5/14	Ｅ
Ｈ０４Ｎ	5/45		Ｈ０４Ｎ	5/45	

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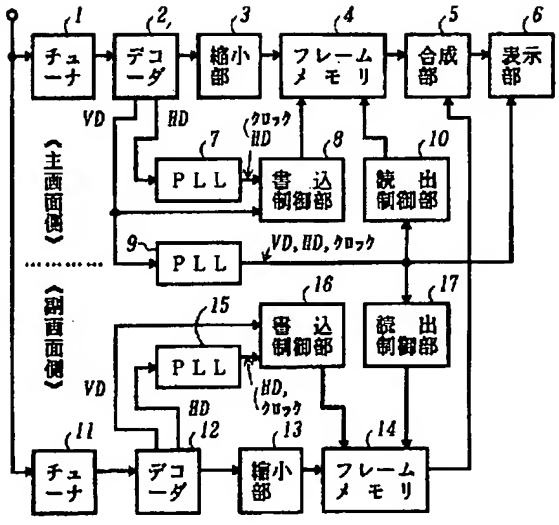
(54)【発明の名称】　マルチ画面表示装置

(57)【要約】

【課題】　マルチ画面の主画面の同期が乱れても副画面の同期が乱されないようにする。

【解決手段】　チューナ１で主画面となる放送を受信し、デコーダ２で分離した映像信号を縮小部３で主画面サイズに縮小し、ＰＬＬ７よりの信号で書込制御部８によりフレームメモリ４に書込み、チューナ11で副画面となる複数の放送を順次受信し、デコーダ12で分離した映像信号をそれぞれ縮小部13で副画面サイズに縮小し、ＰＬＬ15よりの信号で書込制御部16によりフレームメモリ14の所要位置に書込む。デコーダ２よりのHD（垂直同期信号）を基にＰＬＬ９でクロック、HD、VDを生成し、これらの信号を用いて読出制御部10によりフレームメモリ４の信号を、読出制御部17によりフレームメモリ14の信号を読出し、合成部５で合成し、表示部６にマルチ画面を表示する。



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【特許請求の範囲】

【請求項１】　テレビジョン放送を受信するチューナとチューナからの信号をデコードするデコーダとを２組有し、第１のチューナで主画面となる放送を受信し、第１のデコーダよりの映像信号を第１縮小部で所要サイズに縮小し、第１のデコーダで分離された水平同期信号を基に第１ＰＬＬ回路で生成されるクロックと、水平同期信号および第１のデコーダよりの垂直同期信号とにより第１書込制御部を介し第１フレームメモリに書込み、第２のチューナを所要の時間間隔で切換えて副画面となる複数の放送を受信し、第２のデコーダよりの各映像信号を第２縮小部でそれぞれ所要サイズに縮小し、第２のデコーダで分離された水平同期信号を基に第２ＰＬＬ回路で生成されるクロックと、水平同期信号および第２のデコーダよりの垂直同期信号とにより第２書込制御部を介し第２フレームメモリの所要位置にそれぞれ書込み、前記第１フレームメモリより第１読出制御部を介して読出した映像信号、および第２フレームメモリより第２読出制御部を介して読出した映像信号を合成部で合成し表示部によりマルチ画面を表示するものにおいて、前記第１のデコーダよりの垂直同期信号を基にクロックと、水平同期信号および垂直同期信号とを生成する第３ＰＬＬ回路を設け、第３ＰＬＬ回路よりのクロックと、水平同期信号および垂直同期信号とにより第２読出制御部を介し前記第２フレームメモリより映像信号の読出しを行うようにしたマルチ画面表示装置。

【請求項２】　前記第３ＰＬＬ回路よりのクロックと、水平同期信号および垂直同期信号とにより第１読出制御部を介し前記第１フレームメモリより映像信号の読出しを行うようにした請求項１記載のマルチ画面表示装置。

【請求項３】　前記第３ＰＬＬ回路よりのクロックと、水平同期信号および垂直同期信号とにより前記表示部の制御を行うようにした請求項１または２記載のマルチ画面表示装置。

【請求項４】　前記第３ＰＬＬ回路は、前記第１のデコーダよりの垂直同期信号を自走のクロックを基に生成した自走垂直同期信号のタイミングで監視し、第１のデコーダよりの垂直同期信号が判別されない場合、自走のクロックと、自走のクロックを基に生成した水平同期信号および垂直同期信号とを出力するものでなる請求項１、２または３記載のマルチ画面表示装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明はマルチ画面表示装置に係り、主画面となる入力映像信号の同期が乱れた場合に副画面の同期が乱れないようにするものに関する。

【０００２】

【従来の技術】テレビジョン放送を受信するチューナとチューナからの信号をデコードするデコーダとを２組設け、複数画面を同時に表示するマルチ画面表示装置に

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は、図３のブロック図に示す例の如くに構成したものがある。すなわち、チューナ１で主画面となる放送を受信し、デコーダ２で映像信号、水平同期信号(HD)および垂直同期信号(VD)にデコードし、映像信号を縮小部３で縮小し、書込制御部８よりの信号でフレームメモリ４に書込み、同時に、チューナ11で副画面となる複数の放送を所要間隔でチャンネルを切換えて受信し、デコーダ12で映像信号、HDおよびVDにデコードし、映像信号を縮小部13で所要サイズに縮小し、書込制御部16よりの信号でフレームメモリ14の所要位置に順次書込み、読出制御部21および22よりの信号でフレームメモリ４および14より読出した主画面の映像信号および副画面の映像信号を合成部５で合成し、表示部６により表示する。読出制御部21および読出制御部22は、ＰＬＬ回路７にてデコーダ２からのHDに同期させて生成したHDおよびクロックとデコーダ２からのVDとによりフレームメモリ４およびフレームメモリ14からの読出しを行うもので、このため、主画面の同期が乱れたり途切れた場合、デコーダ２からのVDが乱れ、あるいは途切れるため、デコーダ12からの同期信号に乱れがない場合でもフレームメモリ14から読出される信号の同期が乱れ、同時に表示部６の同期が乱されるという問題がある。

【０００３】

【発明が解決しようとする課題】本発明はこのような点に鑑み、副画面の映像信号に同期の乱れがない場合、主画面の映像信号に同期の乱れが生じても少なくともマルチ画面の副画面は同期が乱れずに表示されるようにすることを目的とする。

【０００４】

【課題を解決するための手段】上記目的を達成するため、本発明のマルチ画面表示装置では、テレビジョン放送を受信するチューナとチューナからの信号をデコードするデコーダとを２組有し、第１のチューナで主画面となる放送を受信し、第１のデコーダよりの映像信号を第１縮小部で所要サイズに縮小し、第１のデコーダで分離された水平同期信号を基に第１ＰＬＬ回路で生成されるクロックと、水平同期信号および第１のデコーダよりの垂直同期信号とにより第１書込制御部を介し第１フレームメモリに書込み、第２のチューナを所要の時間間隔で切換えて副画面となる複数の放送を受信し、第２のデコーダよりの各映像信号を第２縮小部でそれぞれ所要サイズに縮小し、第２のデコーダで分離された水平同期信号を基に第２ＰＬＬ回路で生成されるクロックと、水平同期信号および第２のデコーダよりの垂直同期信号とにより第２書込制御部を介し第２フレームメモリの所要位置にそれぞれ書込み、前記第１フレームメモリより第１読出制御部を介して読出した映像信号、および第２フレームメモリより第２読出制御部を介して読出した映像信号を合成部で合成し表示部によりマルチ画面を表示するものにおいて、前記第１のデコーダよりの垂直同期信号を

基にクロック、水平同期信号および垂直同期信号を生成する第３ＰＬＬ回路を設け、第３ＰＬＬ回路よりのクロックと、水平同期信号および垂直同期信号とにより第２読出制御部を介し第２フレームメモリより映像信号の読出しを行う。

【０００５】また、前記第３ＰＬＬ回路よりのクロックと、水平同期信号および垂直同期信号とにより第１読出制御部を介し第１フレームメモリの映像信号の読出しを行う。

【０００６】そして、前記第３ＰＬＬ回路よりのクロックと、水平同期信号および垂直同期信号とにより前記表示部の制御を行う。

【０００７】なお、前記第３ＰＬＬ回路は、第１のデコーダよりの垂直同期信号を自走のクロックを基に生成した自走垂直同期信号のタイミングで監視し、第１のデコーダよりの垂直同期信号が判別されない場合、自走のクロックと、このクロックを基に生成した水平同期信号および垂直同期信号を出力する。

【０００８】

【発明の実施の形態】発明の実施の形態を実施例に基づき図面を参照して説明する。図１は本発明によるマルチ画面表示装置の一実施例の要部ブロック図である。図において、１および11は第１、第２チューナで、第１チューナ１で主画面となるTV放送を受信し、第２チューナ11で副画面となるTV放送を所要の時間間隔で順次チャンネルを切換えて受信する。２および12は第１、第２デコーダで、第１チューナ１または第２チューナ11よりの複合映像信号を処理し、HDおよびVDを分離する。３および13は第１、第２縮小部で、第１デコーダ２または第２デコーダ12よりの映像信号を画素およびラインの間引き等によりそれぞれ所要サイズに縮小する。４および14は第１、第２フレームメモリで、第１縮小部３または第２縮小部13よりの映像信号を書込む。５は合成部で、第１フレームメモリ４および第２フレームメモリ14より読出された映像信号を１画面に合成する。６は表示部で、合成部５よりの信号に基づいてマルチ画面を表示する。７は第１ＰＬＬ回路で、第１デコーダ２よりのHDに同期したクロックを生成し、このクロックを基にHDを生成する。８は第１書込制御部で、第１ＰＬＬ回路７よりのクロック、HDおよび第１デコーダ２よりのVDにより第１フレームメモリ４の書込みを制御する。９は第３ＰＬＬ回路で、第１デコーダ２よりのVDを基準としてクロックを生成し、このクロックを基にHDおよびVDを生成する。10は第１読出制御部で、第３ＰＬＬ回路９よりのクロック、HDおよびVDにより第１フレームメモリ４の読出しを制御する。15は第２ＰＬＬ回路で、第２デコーダ12よりのHDに同期したクロックを生成し、このクロックを基にHDを生成する。16は第２書込制御部で、第２ＰＬＬ回路15よりのクロック、HDおよび第２デコーダ12よりのVDにより第２フレームメモリ14の書込みを制御する。17は第２読出制御部で、第３ＰＬＬ回路９よりのクロック、HDおよびVDにより第２フレームメモリ14の読出しを制御する。

【０００９】次に、本発明によるマルチ画面表示装置の動作を説明する。例えば、図２に示すように主画面と５つの副画面①～⑤とを合成してマルチ画面とする場合、主画面となる放送を第１チューナ１で受信し、第１デコーダ２で映像信号を取出し、第１縮小部３に入力し、ラインおよび画素の間引き等によりライン数および各ラインの画素数をそれぞれ３分の２に縮小し、第１ＰＬＬ回路７よりのクロック、HDおよび第１デコーダ２よりのVDを用いて第１書込制御部８により第１フレームメモリ４の所要位置（図２の主画面に対応する位置）に書込み、第２チューナ11により副画面①、②、③、④、⑤となる各放送チャンネルを所要の時間間隔で順次切換えて受信し、第２デコーダ12でそれぞれ映像信号を取出し、第２縮小部13に入力し、ラインおよび画素の間引き等によりライン数および１ラインの画素数をそれぞれ３分の１に縮小し、第２ＰＬＬ回路15よりのクロック、HDおよび第２デコーダ12よりのVDを用いて第２書込制御部16により第２フレームメモリ14の所要位置（図２の副画面①～⑤に対応する位置）に順次書込みを行う。そして、第１読出制御部10により第１フレームメモリ４より主画面の映像を、第２読出制御部17により第２フレームメモリ14より副画面①～⑤の映像をそれぞれ読出し、合成部５で１画面に合成し、表示部６に入力し画面に表示する。

【００１０】第１、第２読出制御部10、17は、第３ＰＬＬ回路９よりのクロックと、HDおよびVDとを用いてそれぞれのフレームメモリの読出しを行う。第３ＰＬＬ回路９は第２デコーダ２よりのVDを基準にしてクロックを生成し、このクロックを基にHDおよびVDを生成するので、当然、各フレームメモリからの信号の読出し、および表示部６の駆動に同期の乱れは生じないが、第２デコーダ２よりのVDを自走のクロックを基準に生成される自走VDのタイミングで監視しているので、放送波に生じた障害等でVDの周期に乱れが生じ、VD入力が判別されない場合、第１、第２読出制御部10、17に自走のクロックとHDおよびVDとを供給する。従って、第１フレームメモリ４より読出される主画面の信号には同期の乱れがあるのは当然であるが、第２フレームメモリ14の各副画面が同期の正常な状態で書込まれている場合はこれら各副画面は同期の乱れのない状態で読出すことができ、同時にこのクロック等で表示部６を制御するので少なくとも副画面は同期が乱れずに表示される。

【００１１】なお、第２チューナ11は、例えば、副画面①のチャンネル選局時間を副画面②～⑤のチャンネル選局時間より長くし、副画面①は不完全ながら動画で表示し、残る副画面②～⑤はコマ落とし画面で表示するようにする。

【００１２】

【発明の効果】以上に説明したように、本発明によるマ

ルチ画面表示装置によれば、主画面となる映像信号の垂直同期信号を基準としてＰＬＬ回路で生成される同期信号を用いて主・副画面の各フレームメモリからの読出し、および表示部の制御等を行うもので、主画面の同期が乱れた場合でもＰＬＬ回路で自走で生成される同期信号を用いるものであるから、主画面の同期が乱れた場合でも各副画面は同期が乱されずに表示される。

【図面の簡単な説明】

【図１】本発明によるマルチ画面表示装置の一実施例の要部ブロック図である。

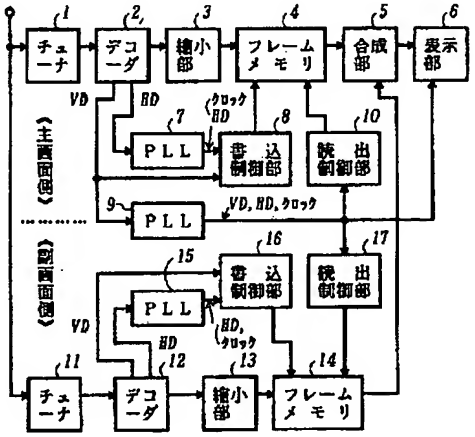
【図２】マルチ画面の一例である。

【図３】従来のマルチ画面表示装置の一例の要部ブロック図である。

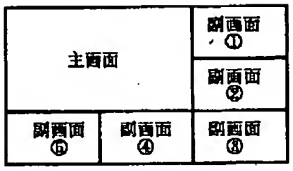
【符号の説明】

1、11　チューナ
2、12　デコーダ
3、13　縮小部
4、14　フレームメモリ
5　合成部
6　表示部
7、9、15　ＰＬＬ回路
8、16　書込制御部
10、17、21、22　読出制御部

【図１】



【図２】



【図３】